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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	ANTHONY M. CHIU
Serial No.	:	09/656,985
Filed	:	September 7, 2000
For	:	SURFACE MOUNT PACKAGE FOR LINEAR ARRAY SENSORS
Group No.	:	2811
Examiner	:	N. Parekh

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
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Sir:

APPELLANTS' BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellants for the application identified above. A check is enclosed for the $320.00 fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC. (f/k/a SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 1–18 are pending in the present application. Claims 8–18 were restricted from claims 1–7 pursuant to 35 U.S.C. § 101 and withdrawn from further consideration. Claims 1–4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,894,707 to *Yamawaki et al* in view of U.S. Patent No. 6,300,169 to *Weiblen et al* and U.S. Patent No. 6,252,252 to *Kunii et al*. Claims 5–7 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all limitations of the base claim and any intervening claim(s). The restriction of pending claims 8–18 and the rejection of pending claims 1–4 are appealed.

STATUS OF AMENDMENTS

No amendments to the claims were submitted following the final Office Action mailed October 11, 2002.

SUMMARY OF THE INVENTION

The present invention relates to forming linear photosensor arrays of the type employed in copies, scanners, fax machines, and the like. Such linear arrays are typically formed within integrated circuit die that are all packaged together, forming a single unit mounted on a circuit board that does not permit repair or replacement of failed, decreasing production yield and often requiring use of redundant linear arrays within a final product. Specification, page 3, line 12 through page 4, line 8.

In the claimed invention, a linear array of a desired length is formed from a plurality of integrated circuits each having photosensors within a portion 302 that will remain exposed after packaging, as well as conductive leads 306 and 308 for soldering to a circuit board:

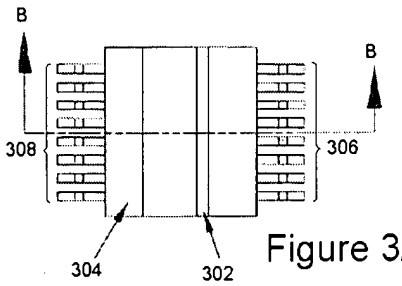


Figure 3A

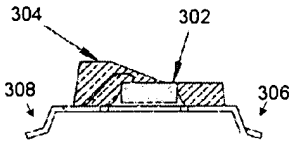


Figure 3B

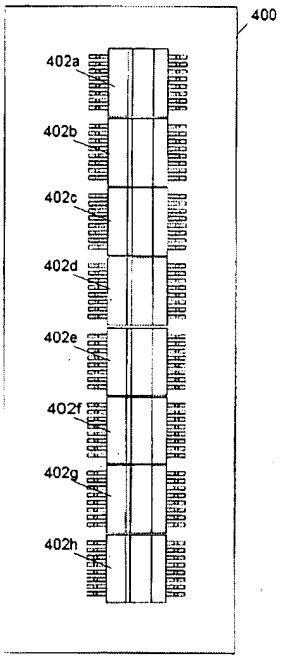


Figure 4

Specification, Figures 3A and 3B, page 10, line 32 through page 11, line 18. To form a linear photosensor array of a desired length, a plurality 402a-402h of the integrated circuits are mounted on a circuit board 400 with the regions containing photosensors in alignment. Specification, Figure 4, page 11, lines 20–26. The individual packages are mounted with minimal spacing, such that dead space along the array may be compensated for by image correction and extrapolation. Specification, page 12, lines 1–16. Preferably leads 306 or 308 on one side of each package are soldered to the circuit board 400, while leads on the other side remain floating to facilitate alignment of the exposed portions 302 within which the photosensors are located. Specification, page 11, lines 11–16 and

page 11, line 28 through page 12, line 1. Any remaining errors in alignment may be compensated by control circuitry, software, or both. Specification, page 11, lines 27–28.

In packaging the integrated circuits, a lead frame strip 102 on which at least one integrated circuit die 104a has been mounted, with bond wires connecting contact pads on the integrated circuit die to portions of the lead frame, is secured to a mold with the integrated circuit and bond wires in the mold cavity in a manner such that a portion 202 of the mold contacts the region within the integrated circuit die 104a in which the photosensors are located, which is the region 302 to remain exposed after packaging:

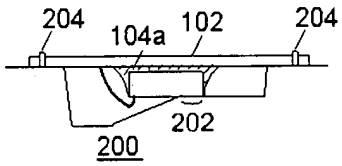


Figure 2

Specification, Figure 2, page 9, line 13 through page 10, line 6. Encapsulating material is injected into the mold cavity. Since the region of the integrated circuit die 104a that contains the photosensors contacts the mold surface 202, that region is not covered by encapsulating material and remains exposed after packaging. A sloped portion of the mold forms a cavity region accommodating the bond wires.

By forming smaller individual photosensor devices mounted in alignment, removal of a particular device for replacement by reflowing solder on the device leads is possible. Yield is

improved and production costs for devices including linear photosensor arrays are reduced, and longer arrays are possible.

ISSUES ON APPEAL

Claims 8–18 were restricted from claims 1–7 pursuant to 35 U.S.C. § 101 and withdrawn from consideration. Claims 1–4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamawaki et al* in view of *Weiblen et al* and *Kunii et al*. The issues on appeal are:

1. Whether claims 8–18 were properly restricted from the application pursuant to 35 U.S.C. § 101; and

2. Whether claims 1–4 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamawaki et al* in view of *Weiblen et al* and *Kunii et al*.

GROUPING OF CLAIMS

Claims 8–18 were restricted from the application pursuant to 35 U.S.C. § 101 and withdrawn from consideration. Claims 1–4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamawaki et al* in view of *Weiblen et al* and *Kunii et al*. For purposes of this appeal, the pending claims will be grouped together as follows:

Group A – claims 8–18;

Group B – claims 1–4;

Group C – claims 3–4; and

Group D – claim 4.

Groups A–D stand or fall independently. Patentability of the claims within each group is argued separately below.

ARGUMENT

Group A

Claims 8–18 were restricted from claims 1–7 pursuant to 35 U.S.C. § 101 and withdrawn from consideration. These claims are properly grouped together and considered separately from the claims of Groups B–D since the claims of Group A are subject to a different grounds of rejection than the claims of Groups B–D.

The Restriction Requirement mailed November 29, 2001 asserted that the method and device claims are distinct based on the contention that the device claims may be manufactured by a materially different process: specifically, that the integrated circuit devices may be packaged after being mounted on the circuit board.

Restriction is only proper where the claims are independent or distinct. MPEP § 806. In passing on questions of restriction, the claimed subject matter must be compared in order to determine distinctness and independence. MPEP § 806.01. Pending independent method claim 1 does not recite packaging the integrated circuit, only that the integrated circuits each include a linear array of photosensors within a portion remaining exposed after packaging. Method claims 2 and 6 recite packaging the integrated circuits, but do not specify whether the integrated circuits are packaged before or after being mounted on the circuit board. Restricted independent claims 8, 13

and 17 are structure claims that do not contain any limitations regarding when packaging occurs. Accordingly, the restriction requirement has no basis in the claims.

In addition, a process of making and the product made are distinct inventions only if: (A) the process as claimed is not an obvious process of making the product and can be used to make other and different products; and (B) the product as claimed can be made by another and materially different process. The Restriction Requirement asserts that packaging the integrated circuits after they are mounted on the circuit board is materially different than packaging the integrated circuits before they are mounted on the circuit board. However, no evidence of record supports the assertion that packaging the integrated circuits before they are mounted on the circuit board was, at the time the application was filed, patentably distinct from packaging the integrated circuits after they are mounted on the circuit board. In addition, the record contains no evidence that packaging the integrated circuits after they have been mounted on the circuit board is even possible. The restriction is thus arbitrary and capricious for both reasons.

Group B

Claims 1–4 of Group B were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamawaki et al* in view of *Weiblen et al* and *Kunii et al*. These claims are properly grouped together and considered separately from the claims of Groups A and C–D because the claims of Group B are subject to a different grounds of rejection than the claims of Group A and because a favorable

decision with respect to the claims of Group B may obviate the need for consideration of the claims of Groups C–D.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to

modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

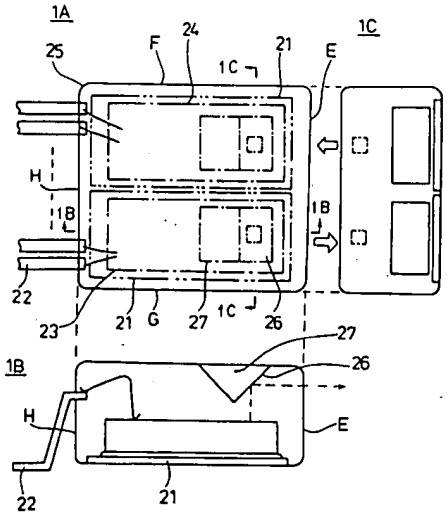
Independent claim 1 of Group B recites forming a plurality of integrated circuits each having a linear array of photosensors therein and conductive leads, then mounting the integrated circuits on a printed circuit board with the photosensors in alignment, with at least some leads for each integrated circuit soldered to the circuit board. Such a feature is not found in the cited references. *Yamawaki et al* depicts and described only a single semiconductor chip 1 for a motion video camera with a light detection section 4 having 200,000 to 400,000 light sensors within a square 10 microns wide. *Yamawaki et al*, column 1, line 51–55. *Yamawaki et al* is silent as to mounting a plurality of such semiconductor chips on a circuit board with the light detection sections in alignment.

The cited portion of *Weiblen et al* depicts a lead grid 10 with an array of lead frames for mass-production, concurrent packaging of multiple semiconductor pressure sensing elements 2 each including a semiconductor chip 3. *Weiblen et al*, column 2, lines 46–60. However, *Weiblen et al* specifies that individual units are separated prior to transfer molding packaging of pressure sensing elements 2 affixed to different lead frames within the lead grid 10. *Weiblen et al*, column 3, lines 8–16. *Weiblen et al* is silent as to mounting the packaged pressure sensors on a circuit board with

the pressure sensors in alignment, or packaging the pressure sensors without separation from the lead grid 10 then mounting the entire lead grid on a printed circuit board. In addition, *Weiblen et al* is not an analogous reference to the claimed invention. In order to rely on a reference as a basis for an obviousness rejection, the rejection must be analogous to the claimed invention--that is, either within the field of endeavor of the invention or reasonably pertinent to the problem with which the invention is concerned. MPEP § 2141.01(a). *Weiblen et al* does not relate to photosensors, formation of long photosensors by mounting shorter photosensors in alignment, or even mounting integrated circuits on circuit board, but instead relates only to mass-production packaging of pressure sensors.

Kunii et al discloses one light emitting element 23 and one light sensing element 24 mounted side-by-side on an island 21 and packaged together with wire bond connections to leads 22:

FIG. 1



Kunii et al, Figure 1, column 7, lines 40–61. The package 50 is then mounted on a printed circuit board 48:

FIG. 9

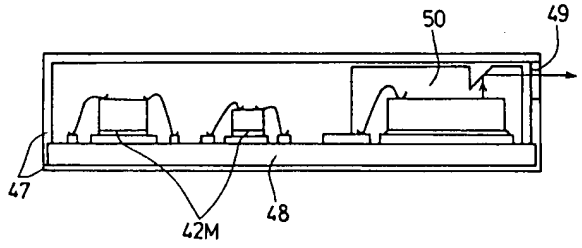
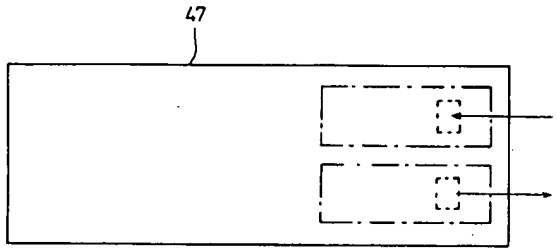


FIG. 10



Kunii et al, Figures 9 and 10, column 12, lines 1–14. In an alternative embodiment, the light emitting element 23 and the light receiving element 24 are mounted directly on a printed circuit board 41. *Kunii et al*, Figure 6, column 11, lines 1–8. However, the light emitting element 23 in *Kunii et al* cannot reasonably be characterized as a "photosensor" within the ordinary meaning of that term. Thus, the combination of light emitting element 23 and light sensing element 24 depicted and described in *Kunii et al* fails to satisfy the limitation of a plurality of integrated circuits each having photosensors. In addition, independent claim 1 of Group B recites integrated circuits each having a linear array of photosensors therein, which is not satisfied by the single light emitting or light receiving elements 23 and 24 depicted and described in *Kunii et al.*

Accordingly, the claim limitation of a plurality of integrated circuits each having a linear array of photosensors therein and conductive leads, mounted on a printed circuit board with the

photosensors in alignment and at least some leads for each integrated circuit soldered to the circuit board, is not found in the cited references, taken alone or in combination.

Group C

Claims 3–4 of Group C were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamawaki et al* in view of *Weiblen et al* and *Kunii et al*. This claim is properly considered separately from the claims of Groups A, B and D because (a) the claims of Group C are subject to a different grounds of rejection than the claims of Group A, and (b) the claims of Group C contain a common limitation distinguishing the claimed invention over the cited references that is not found in the claims of Groups B and D.

Claims 3–4 of Group C each recite packaging the individual integrated circuits using a mold, with the portion of the integrated circuit die to remain exposed after packaging (i.e., the region containing the photosensors) in contact with the mold to prevent encapsulating material from adhering to that portion. Such a feature is not found within the cited references, taken alone or in combination.

Group D

Claim 4 of Group D was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamawaki et al* in view of *Weiblen et al* and *Kunii et al*. This claim is properly considered separately from the claims of Groups A–C because (a) the claim of Group D is subject to a different grounds of rejection than the claims of Group A, and (b) the claim of Group D contains a limitation

distinguishing the claimed invention over the cited references that is not found in the claims of Groups B–C.

Claim 4 of Group D recites packaging the individual integrated circuits using a mold with a sloped surface adjacent to the portion of the mold contacting the integrated circuit die where the photosensors are located. Such a feature is not found within the cited references, taken alone or in combination. None of the cited references depicts or describes a packaging mold having a surface contacting the integrated circuit die, or a sloped surface adjacent to such portion.

CONCLUSION

The restriction of the claims of Group A has no basis in the claims and is unsupported by any evidence of record. Therefore, the restriction under 35 U.S.C. § 101 is improper. None of the cited references, taken alone or in combination, depict or describe all features of the invention claimed in Groups B–D. Therefore, the rejection under 35 U.S.C. § 103 is improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below restricting pending claims 8–18 from the application and rejecting pending claims 1–4 in the application.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 5-19-03

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APPENDIX TO APPELLANT'S BRIEF ON APPEAL
PENDING CLAIMS ON APPEAL

1. (unchanged/original) A method of forming a linear photosensor array, comprising:

forming a plurality of integrated circuits each including a linear array of photosensors within a portion of the integrated circuit remaining exposed after packaging and a plurality of conductive leads adapted for soldering to a circuit board;

mounting the integrated circuits with the portions containing the photosensors in alignment on a circuit board; and

soldering at least some of the leads for each integrated circuit to the circuit board.

2. (unchanged/original) The method of claim 1, wherein the step of forming a plurality of integrated circuits each including a linear array of photosensors within a portion of the integrated circuit remaining exposed after packaging and a plurality of conductive leads adapted for soldering to a circuit board further comprises:

packaging each of the plurality of integrated circuit packages by:

affixing an integrated circuit die to a lead frame;

connecting the integrated circuit die to selected portions of the lead frame with bond wires; and

encapsulating a portion of the lead frame and the integrated circuit die except for the exposed region, wherein the exposed region of the integrated circuit die remains exposed to external ambient light.

3. (unchanged/original) The method of claim 2, wherein the step of encapsulating a portion of the lead frame and the integrated circuit die except for the exposed region, wherein the exposed region of the integrated circuit die remains exposed to external ambient light further comprises:

after affixing the integrated circuit die to the lead frame and connecting the bond wires, mounting the lead frame with the integrated circuit die and bond wires in a mold with a portion of the mold in contact with the exposed region of the integrated circuit die to prevent encapsulating material from adhering to the exposed region of the integrated circuit die.

4. (unchanged/original) The method of claim 3, wherein the step of mounting the lead frame with the integrated circuit die and bond wires in a mold with a portion of the mold in contact with the exposed region of the integrated circuit die to prevent encapsulating material from adhering to the exposed region of the integrated circuit die further comprises:

mounting the lead frame with the integrated circuit die and bond wires in a mold having a sloped surface adjacent to the portion of the mold contacting the exposed region of the integrated circuit die, wherein the sloped surface forms one surface of a mold cavity receiving the bond wires when the lead frame with the integrated circuit die is mounted in the mold.

5. (unchanged/original) The method of claim 1, wherein the step of forming a plurality of integrated circuits each including a linear array of photosensors within a portion of the integrated circuit remaining exposed after packaging and a plurality of conductive leads adapted for soldering to a circuit board further comprises:

mounting a plurality of integrated circuit die on a lead frame strip with a separation between the mounted integrated circuit die approximately equal to a kerf width for a singulation saw to be used in separating the packaged integrated circuits.

6. (unchanged/original) The method of claim 1, wherein the step of mounting the integrated circuits with the portions containing the photosensors in alignment on a circuit board further comprises:

packaging the integrated circuits with the portion containing the photosensors exposed; and

mounting adjacent packaged integrated circuits in contact with each other.

7. (unchanged/original) The method of claim 1, wherein the step of soldering at least some of the leads for each integrated circuit to the circuit board further comprises:

soldering only leads on one side of each integrated circuit to the circuit board, leaving leads on an other side of the packaged integrated circuits in floating contact with conductive structures on the circuit board to facilitate adjustment and removal of integrated circuits.

8. (original/withdrawn) An integrated circuit package for a linear photosensor array, comprising:

a lead frame including a die paddle and a plurality of leads;

an integrated circuit die affixed to the die paddle, the integrated circuit die including a plurality of photosensitive devices linearly aligned along a length of an upper surface of the integrated circuit die; and

packaging encapsulating a portion of the lead frame and the integrated circuit die except for a region of the integrated circuit die containing the photosensitive devices, wherein the region containing the photosensitive devices remains exposed through the packaging.

9. (original/withdrawn) The integrated circuit package of claim 8, wherein the die paddle of the lead frame is shorter than the integrated circuit die.

10. (original/withdrawn) The integrated circuit package of claim 8, wherein the integrated circuit is affixed to the lead frame with an adhesive.

11. (original/withdrawn) The integrated circuit package of claim 8, wherein the packaging does not cover ends of the integrated circuit die.

12. (original/withdrawn) The integrated circuit package of claim 8, further comprising:

bond wires connecting the integrated circuit die to selected portions of the lead frame, wherein the packaging encapsulated the bond wires.

13. (original/withdrawn) A linear photosensor array, comprising:

a circuit board; and

a plurality of packaged integrated circuits mounted on the circuit board, wherein each packaged integrated circuit includes an array of photosensors linearly aligned along a length of a surface region of an integrated circuit die therein and a plurality of conductive leads adapted for soldering to the circuit board,

wherein the packaged integrated circuits are mounted in a line on the circuit board with the surface regions of each packaged integrated circuit in alignment, and

wherein at least some of the leads for each packaged integrated circuit are soldered to the circuit board.

14. (original/withdrawn) The linear photosensor array of claim 13, wherein the each of the integrated circuit packages further comprises:

an integrated circuit die affixed to a lead frame;

bond wires connecting the integrated circuit die to selected portions of the lead frame; and

packaging encapsulating a portion of the lead frame, the integrated circuit die except for the surface region containing the array of photosensors and ends of the integrated circuit die, and the bond wires,

wherein the surface region of the integrated circuit die containing the array of photosensors remains exposed to ambient light.

15. (original/withdrawn) The linear photosensor array of claim 13, wherein adjacent packaged integrated circuits on the circuit board are mounted in contact with each other such that the array of photosensors on each integrated circuit die form a single, long, continuous photosensor array.

16. (original/withdrawn) The linear photosensor array of claim 13, wherein only leads on one side of each packaged integrated circuit mounted on the circuit board are soldered to the circuit board, while leads on an other side of each packaged integrated circuit are left in floating contact with conductive structures on the circuit board to facilitate adjustment and removal of packaged integrated circuits.

17. (original/withdrawn) A mold for packaging integrated circuits, comprising:

a surface against which a lead frame strip may be placed, the surface including pins projecting therefrom which are received by tooling holes within a lead frame strip placed against the surface;

a plurality of cavity regions extending from the surface, each cavity region receiving an integrated circuit die affixed to the lead frame strip and bond wires connecting the integrated circuit die to the lead frame strip when the lead frame strip is placed against the surface, each cavity region formed by:

a first surface contacting a surface region of the integrated circuit die when the lead frame strip is placed against the surface and preventing encapsulate material from adhering to the surface region of the integrated circuit die, and

a sloped surface extending from the first surface of the cavity to form an area receiving the bond wires connecting the integrated circuit die to the lead frame strip when the lead frame strip is placed against the surface.

18. (original/withdrawn) The mold of claim 17, wherein the plurality of cavity regions are contiguous and form a single cavity.